44. (New) The memory system as in Claim 43, wherein each of the plurality of T-RAM cells further comprises a transfer gate portion.

45. (New) The memory system as in Claim 44, wherein each of the transfer gate portions of the plurality of T-RAM cells comprise a halo region of a single polarity.

46. (New) The memory system as in Claim 45, wherein the single polarity halo region of the transfer gate portions of each of the plurality of T-RAM cells is fabricated in the same steps as one of the halo regions of the thyristor portion.

47. (New) The memory system as in Claim 43, wherein the plurality of T-RAM cells have a planar cell structure.

48. (New) The memory system as in Claim 43, wherein each of the plurality of T-RAM cells have at least one support device associated therewith.

49. (New) The memory system as in Claim 48, wherein the at least one support device associated with each of the plurality of T-RAM cells is fabricated simultaneously with fabrication steps for fabrication of the T-RAM cells.

50 (New) The memory system as in Claim 48, wherein each of the plurality of T-RAM cells has a first support device and a second support device associated therewith.

51. (New) The memory system as in Claim 50, wherein the first support device is a p-MOS support device and the second support device is an n-MOS support device.

52. (New) The memory system as in Claim 51, wherein the p-MOS support device comprises an n-type halo region and the n-MOS support device comprises a p-type halo region.

53. (New) The memory system as in Claim 52, wherein the n-type halo region of the p-MOS support device is fabricated simultaneously with fabrication steps for fabrication of one of the halo regions of the T-RAM cells and the p-type halo region of the n-MOS support device is fabricated simultaneously with fabrication steps for fabrication of the other halo region of the T-RAM cells.

54. (New) The memory system as in Claim 43, wherein the two halo regions of the T-RAM cells having different polarities form a contiguous halo region having two portions with different polarities.

55. (New) The memory system as in Claim 43, wherein each of the halo regions having different polarities is adjacent to a respective source/drain region associated the thyristor, the polarity of each source/drain region being opposite that of the adjacent halo region.

56. (New) A method for fabricating a multiplicity of T-RAM cells in an array on a semiconductor wafer, the method comprising:

fabricating a plurality of T-RAM cells, each T-RAM cell comprising a thyristor portion, the fabrication of the thyristor portion of each T-RAM cell including creating a first halo region of a first polarity type and a second halo region of a second polarity type.

57. (New) The method as in Claim 56, wherein the first halo region and the second halo region are created to form one contiguous halo region for the thyristor portion.

58. (New) The method as in Claim 56, wherein creating the first halo region comprises providing a first mask to the thyristor portion of each T-RAM cell, the first mask covering a second portion of the thyristor portion and leaving a first portion of the thyristor portion unmasked, and providing a halo implant of the first polarity type to the

first portion of the thyristor portion of each T-RAM cell, the first portion corresponding at least in part to the first halo region.

59. (New) The method as in Claim 58, wherein, prior to providing the halo implant of the first polarity type to the first portion, an extension implant of the second polarity type is provided to the first portion.

60. (New) The method as in Claim 58, wherein the first mask further leaves a transfer gate portion of each of the plurality of T-RAM cells unmasked, the halo implant of the first polarity type also being provided to the entire transfer gate portion of each of the plurality of T-RAM cells.

61. (New) The method as in Claim 58, wherein creating the second halo region comprises providing a second mask to the thyristor portion of each T-RAM cell, the second mask covering the first portion of the thyristor portion and leaving the second portion of the thyristor portion unmasked, and providing a halo implant of the second polarity type to the second portion of the thyristor portion of each T-RAM cell, the second portion corresponding at least in part to the second halo region.

62. (New) The method as in Claim 61, wherein, prior to providing the halo implant of the second polarity type to the second portion, an extension implant of the first polarity type is provided to the second portion.

63. (New) The method as in Claim 61, wherein creating the second halo region further comprises a second providing of the second mask to the thyristor portion of each T-RAM cell, the second mask again covering the first portion of the thyristor portion and leaving the second portion of the thyristor portion unmasked, and providing an implant of the first polarity type to the second portion of the thyristor portion of each T-RAM cell, the second halo region being formed upon application of the implant of the first polarity type.

64. (New) The method as in Claim 63, wherein creating the first halo region further comprises a second providing of the first mask to the thyristor portion of each T-RAM cell, the first mask again covering the second portion of the thyristor portion and leaving the first portion of the thyristor portion unmasked, and providing an implant of the second polarity type to the first portion of the thyristor portion of each T-RAM cell, the first halo region being formed upon application of the implant of the second polarity type.

65. (New) The method as in Claim 58, wherein the first mask further leaves a transfer gate portion of each of the plurality of T-RAM cells unmasked, the halo implant of the first polarity type also being provided to the entire transfer gate portion of each of the plurality of T-RAM cells.

## REMARKS

This amendment is submitted in response to the Office Action dated December 6, 2001. Claims 1-42 have been cancelled above without prejudice and new Claims 43-65 have been inserted. Since new Claims 43-65 are now pending in the application, it is submitted that the prior election/restriction requirement given for Claims 1-42 in paragraphs 2-7 of the Office Action is no longer applicable. It is further submitted that an election/restriction requirement is not applicable for current Claims 43-65 under the standard given in paragraph 3 of the Office Action.

In response to the drawing objection in paragraphs 8 and 9 of the Office Action, a proposed correction to Fig. 13 is submitted herewith. A revised formal drawing will be sent after approval of the correction and allowance of the application by the Examiner.

In paragraphs 12 and 13 of the Office Action, now cancelled Claims 1-13 were rejected under 35 U.S.C. 103(a) as being unpatentable of U.S. Patent No. 6,229,161 to Nemati et al. in view of U.S. Patent No. 5,945,715 to Kuriyama.

New independent Claim 43 recites "A memory system comprising a plurality of T-RAM cells arranged in an array, each of the plurality of T-RAM cells comprising a thyristor portion having two halo regions having different polarities". Independent Claim 56 has analogous recitations. Among other things, two halo implant regions having